Annealing effects on electrical properties and defects of $CaCu_3Ti_4O_{12}$ thin films deposited by pulsed laser deposition

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(Received 28 March 2010; revised manuscript received 10 May 2010; published 21 June 2010)

A systematic study was carried out to assess property changes in $CaCu_3Ti_4O_{12}$ thin films upon annealing in air in order to evaluate the impact of oxygen vacancies on their colossal dielectric constant behavior. Highly preferentially oriented thin-film samples were deposited by pulsed laser deposition method at 720 °C in 200 mTorr oxygen. The as-deposited thin films show the typical feature of colossal dielectric constant. Annealing experiments were conducted at 480, 580, 620, and 680 °C with intermediate electrical measurements. The evolutions of the electrical properties (such as, dielectric constant, loss, resistance, etc.), defect concentration and activation energy, were observed with the increase in the annealing temperature. Capacitance-temperature results exhibited the double-plateau feature in the measuring temperature range, revealing two defect levels in the sample. The activation energy and concentration of these two defects were estimated at each annealed state. The sensitivity of these defects to oxygen atmosphere confirmed our previous conclusion about oxygen vacancies as the chemical origin of the colossal dielectric constant phenomenon in $CaCu_3Ti_4O_{12}$. Numerical simulation to the capacitance response of a Schottky junction with two defects supports the experimental results. Annealing at 680 °C changed the sample from the colossal dielectric state into a normal dielectric state with a negative temperature coefficient of dielectric constant. In such a fully annealed state, the intrinsic dielectric properties of $CaCu_3Ti_4O_{12}$ were observed. The abnormal increase in dielectric constant at low temperature may be attributed to the magnetodielectric coupling caused by magnetic ordering.

DOI: 10.1103/PhysRevB.81.224111 PACS number(s): 77.22.Gm, 73.20.Hb

I. INTRODUCTION

As the first colossal dielectric constant (CDC) material,[1] $CaCu_3Ti_4O_{12}$ (CCTO) still attracts intensive scientific interests due to the unsatisfying elucidation of its CDC phenomenon. CDC behavior has been observed in various CCTO samples, from ceramics to single crystals to thin films, regardless of the producing methods.[2–6] Different models have been proposed to explain this phenomenon such as twin boundary model,[7] internal barrier layer capacitor (IBLC) model,[4] surface layer model,[8] and so on. A Maxwell-Wagner effect proposed in the IBLC model[4] and surface layer model[8] has been widely accepted to explain the CDC phenomenon observed in polycrystalline CCTO samples. For those samples without grain boundaries as the insulating barrier, for example, single crystals, however, new models should be proposed to understand the underlying mechanism. On the basis of experiments, recently, we proposed a depletion layer capacitance model to explain the observed CDC phenomenon in CCTO thin films.[9] This model is suitable for cases without grain boundaries since it attributed CDC to the sample-electrode interfaces. Even though these efforts gave us a contour of the underlying physical mechanism of CDC, there are still many open questions. The relatively large optical band gap of over 2.8 eV (Ref. 10) would not allow conduction at room temperature (RT) and even below RT if the material is of intrinsic conduction. Without doping, there must be some intrinsic defects in CCTO lattices. Which types of defects change CCTO into conductive? What are the energy levels of these defects? No matter which synthesis procedure was used, why could these defects not be avoided? What are the intrinsic dielectric properties of CCTO? All these questions are important to understand the whole story about CDC and CCTO.

Measuring capacitance as a function of temperature on Schottky junctions is a powerful technique to investigate defects in semiconductors. This technique has been widely used to determine the defect levels in the III-V semiconductors[11] and the principle of the technique is well understood. Several models have been proposed to simulate the capacitance variation with temperature and frequency. For example, Losee[12]applied a numerical simulation technique to determine impurity levels in Au-ZnTe samples by simulating the measured capacitance data. Vincent *et al.*[11] built a simple effective model to simulate the capacitance and conductance as functions of temperature and frequency. This model gave quite reasonable explanation to their measured data in GaP. Different from those brick-layer models based on *RC* networks, these models concern more about physical processes, such as carrier freeze-out, charge capture and emission at deep defect levels, and so on. In order to reveal more details about the relaxation mechanism in CCTO, we adopted Vincent's model to simulate the capacitance behavior as a function of temperature.

Our recent research work showed that CDC phenomenon is suppressed or quenched by annealing CCTO thin-film samples at certain conditions.[6] This indicated that annealing is an effective way to reduce defects in CCTO. Thus, it is interesting to systematically investigate annealing effects on electrical properties of CCTO samples. In this paper, we present a systematic study of electrical properties of CCTO thin films after multiple annealing procedures. The evolution of defect concentrations, energy levels with annealing temperatures will be shown. Intrinsic dielectric properties of CCTO will be presented as well.

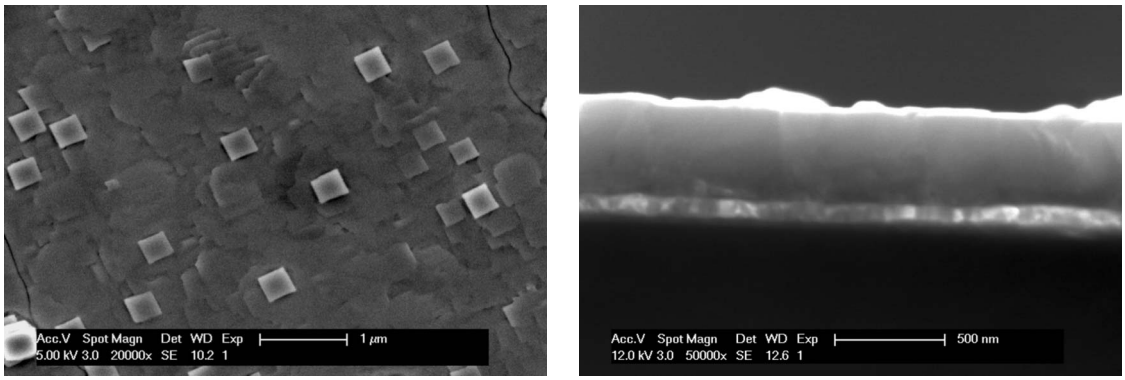

FIG. 1. (a) Typical surface morphology and (b) cross-sectional SEM images of CCTO thin films.

II. EXPERIMENT

The CCTO thin-film sample for this study was deposited by our pulsed laser deposition system, which was equipped with a KrF excimer laser (Lambda Physics) emitting at 248 nm with pulse duration of 25 ns. The target was a pure phase dense CCTO ceramic target synthesized by solid-state reaction. The CCTO thin films were directly grown on stabilized $Pt/TiO_2/Ti/SiO_2/Si(100)$ substrates at a substrate temperature of ~720 °C under 200 mTorr oxygen pressure. At a target-substrate distance of 5.0 cm, the thin film was grown for 90 min with a repetition rate of 5 Hz and a fluency of 220 mJ. After deposition, the film was annealed at the same oxygen pressure for 10 min before cooling to RT. Pt electrodes (~150 μm in diameter) were sputtered on the top of the sample to form sandwich-structure capacitors for electrical measurements by using a mask and an EMS 575 XD Turbo Sputter Coater. Subsequently, the samples were annealed at 480, 580, 620, and 680 °C in air for 10 h. Electrical properties were assessed in the as-deposited state and after each annealing step. The temperature dependence of dielectric constant, the capacitance-voltage (C-V) curves, and the impedance spectra were measured on a HP 4284 an impedance analyzer connected with a MMR K20 microrefrigerator. The current-voltage (I-V) curves were measured using Keithley 617 programmable electrometer. Phase purity of all the as-deposited and as-annealed samples was checked by x-ray diffraction experiments on an x-ray diffractometer of Siemens D500. The surface and cross-sectional morphologies of the CCTO thin-film samples were observed under scanning electron microscopy (SEM) and transmission electron microscopy (TEM) (Philips XL30 ESEM and Philips CM 20 TEM), showing a dense and columnar microstructure [see Figs. 1(a) and 1(b)]. No intermediate grain boundaries in parallel with the top or bottom electrode can be seen. The film thickness amounted to ~410 nm.

III. RESULTS AND DISCUSSIONS

A. Electrical properties of the as-deposited sample

Figure 2 depicts the temperature dependency of the dielectric response of the as-deposited sample. The ε_r-T curves show two plateaus in the measuring temperature range from 80 to 320 K. The plateau ε_r values at low-temperature and high-temperature ends are ~150 and ~1800 (100 kHz), respectively. The so-called low-temperature relaxation process took place at ~120 K, similar to that reported in a CCTO single crystal.[2] This relaxation shows up as the low-temperature peaks in the temperature dependency curves of dielectric loss in Fig. 2(b). The activation energy for this relaxation process was derived to be E_a=87 meV, consistent with the reported values for single crystals,[2,4] indicating that the same defect is responsible for this relaxation process.

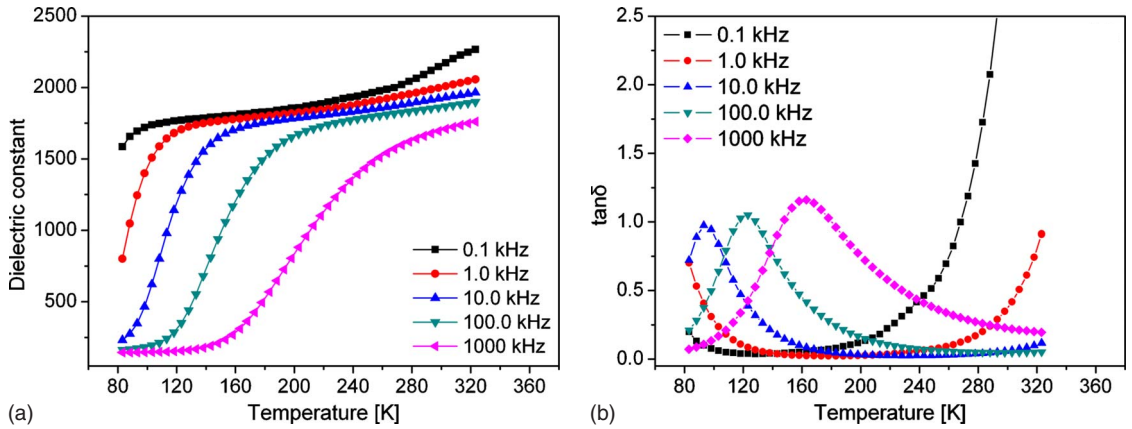

FIG. 2. (Color online) Temperature dependencies of (a) dielectric constant and (b) loss of the as-deposited CCTO thin film.

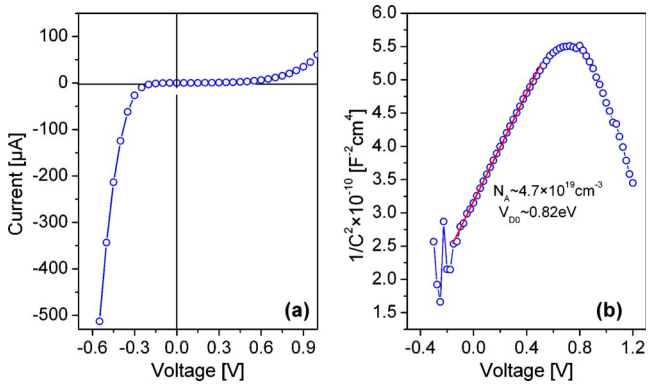

FIG. 3. (Color online) (a) I-V curve and (b) C^{-2}-V curve of the as-deposited CCTO thin film.

The I-V and C-V results show typical features of metal-semiconductor (MS) Schottky junction, as shown in Fig. 3. The I-V curve is nonlinear and asymmetric, and C^{-2}-V curve exhibits a linear relationship at small positive biases. The I-V nonlinearity can be attributed to the Schottky barrier at the top electrode interface. According to semiconductor theory, the depletion capacitance of an MS junction with a homogeneous doping has the following relationship with the biased voltage (V):[13]

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_S N_A^-}(\Phi - V), \tag{1}$$

where C is the capacitance, Φ the Schottky barrier height, q the electronic charge, ε_S the semiconductor dielectric constant, and N_A^- the ionized acceptor concentration. As can be seen from Eq. (1), the MS capacitance minimizes at low temperature due to the carrier freeze-out (e.g., very small N_A^-). On heating, the carriers are activated, consequently resulting in high N_A^- and capacitance. At temperature higher than the activation temperature, the carriers keep constant thanks to the fully ionized defects. Thus, capacitance shows a plateau value with the variation in temperature. These temperature-dependent features just correspond to the capacitance curves in Fig. 2(a). In Fig. 3(b), the measured C^{-2}-V curve can be well fitted to a straight line at low-voltage ranges, meaning that the junction was a standard MS junction. And the impurity density was derived to be $\sim 4.7 \times 10^{19}$ cm^3, using a relative dielectric constant of 75 for CCTO. This value is close to the previous reported concentrations in the CCTO thin-film samples.[14] The calculated Schottky barrier height is ~ 0.82 eV, which is quite consistent with the reported values in CCTO thin films (0.6–0.8 eV) (Ref. 9) and in fact quite close to the activation energy of the barrier layer in ceramics (0.77 eV).[15]

B. Annealing effects on electrical properties

Figure 4 shows the temperature dependencies of dielectric constant and loss after the sample annealing at 480 °C. The dielectric constant was substantially decreased in the whole temperature range. From ~ 120 to ~ 240 K, the measured dielectric constant is only ~ 400, much lower than the value of 2000 in the as-deposited sample. At temperature higher than ~ 240 K, the dielectric constant increases gradually on heating, which means that another defect mechanism starts to play a role in conduction. However, no saturation was detected in the measuring temperature range. The dielectric loss in Fig. 4(b) shows the corresponding low-temperature relaxation peaks below 220 K, shifting from low to high temperature with the increase in measuring frequencies. The dielectric loss curves show some signs of the second relaxation at relative higher temperature—very weak peaks, which can be observed at high frequencies and were covered by the large loss background at low frequencies. From Eq. (1), we know that the capacitance is proportional to the square root of the ionized defect concentration. Thus, we speculate that these low and high-temperature relaxations must be assigned to the excitations of two different defects, a shallow and deep one corresponding to the low (denoted as D_{LT}) and high (denoted as D_{HT}) temperature relaxations, respectively. Similar two-step capacitance plateaus were observed in the capacitance-temperature curves of GaAs, which contained two deep traps.[16] Comparing with this annealed sample, the as-deposited sample show a quite weak second relaxation in the dielectric measurement. The reason could be that D_{LT} has much higher concentration than D_{HT} and is overwhelming in the electrical response.

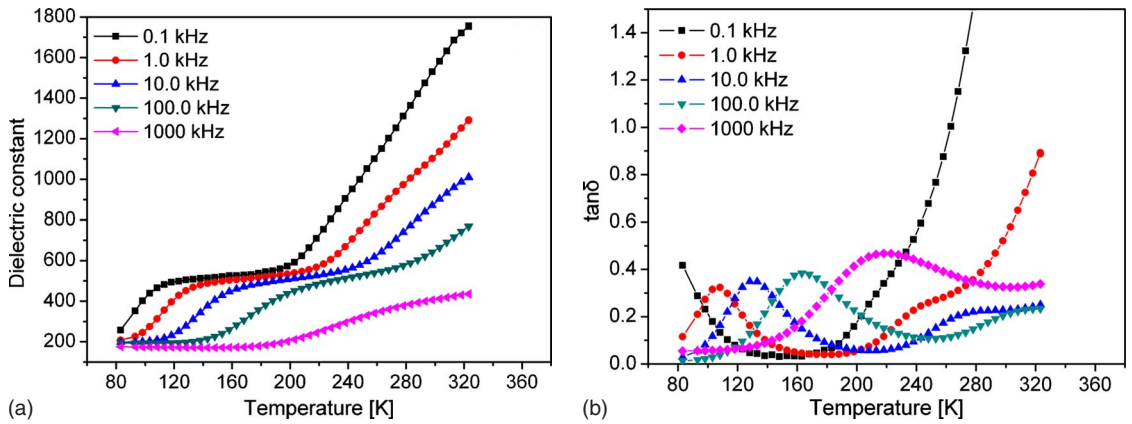

FIG. 4. (Color online) Temperature dependencies of (a) dielectric constant and (b) loss of the CCTO thin film annealed at 480 °C.

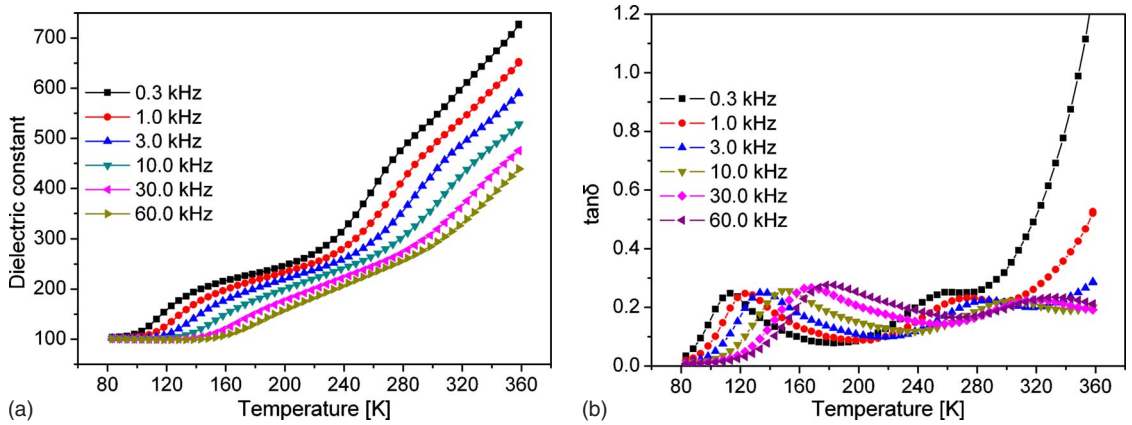

FIG. 5. (Color online) Temperature dependencies of (a) dielectric constant and (b) loss of the CCTO thin film annealed at 620 °C.

No evident change was observed after annealing at 580 °C for 10 h (the results are not shown here). The dielectric constant did not decrease at the low-temperature range (80–200 K) but apparently decreased at the high-temperature range (200–320 K). This means that D_{LT} was sensitive to the annealing below 480 °C and became stable after the first annealing step. Contrarily, even though D_{HT} was not much influenced by annealing at 480 °C, its concentration was apparently suppressed by annealing at 580 °C.

The most interesting results were obtained after annealing at 620 °C and are shown in Fig. 5. The ε_r-T curves in Fig. 5(a) exhibit a more pronounced two-step relaxation at low- and high-temperature ranges, respectively. The dielectric constant substantially decreased to ~190 for the low-temperature range and 600–700 at the high-temperature range. Even though the annealing temperature increased only by 50 °C, these values are much lower than those measured after annealing at 580 °C. Similarly, the dielectric losses in Fig. 5(b) are much lower than the previous values in the entire temperature range. The most striking feature for these curves is that all of them contain two peaks, which correspond to the two relaxations at low and high temperatures. The activation energy of these two relaxation processes can be deduced from the relationship between the relaxation time τ and the reversal of temperature $(1/T)$, as shown in Fig. 6. The E_a values were calculated to be ~0.15 and ~0.58 eV for the low- and high-temperature processes, respectively. It is worthwhile to notice that E_a of D_{LT} increased from 0.085 to 0.15 eV by raising the annealing temperature.

As shown in Fig. 7, a completely different dielectric behavior was observed after annealing at 680 °C. The dielectric constant shows a value between 160 and 170 at the low-temperature range, having a negative slope as a function of temperature in the range from ~80 to ~160 K. The low dielectric constant, as well as the negative slope, is consistent with the reported dielectric constant measured in the far-infrared frequency band.[2,17] This is the first time to measure such kinds of electrical properties in pure CCTO at radio frequencies. The negative temperature dependence of dielectric constant could be attributed to two possibilities: incipient ferroelectricity[18] or magnetodielectric coupling.[19] As shown in the inset of Fig. 7, a linear relationship between $1/\varepsilon_r$ and T can be obtained at the temperature range from 83 to 140 K, hinting a Curie-Weiss behavior and incipient ferroelectricity. Curie temperature and constant were derived to be −2852 K and 44 452 K, respectively. Similar Curie-Weiss behavior was found in Mn-doped CCTO ceramics.[20] However, since CCTO undergoes an antiferromagnetic transition at ~25 K, another possibility for the negative ε_r-T curve is the magnetodielectric coupling effect at $T > T_N$.[19] As shown in Fig. 7(b), the dielectric losses are quite low even at the elevated temperature range, different from the rapid increase feature of those loss data before this annealing step. This difference indicates that the dc leakage has been efficiently suppressed after annealing at 680 °C. Namely, the long-range conduction was prohibited. However, the high-frequent dielectric losses are higher than the low-frequent ones, indicating the corresponding local ac conductivity still exist in the annealed sample. This can be also used to explain the increase in dielectric constant at high frequencies, especially at high temperatures.

Figure 8(a) shows the I-V curves of the as-deposited and annealed samples. The current density substantially decreased after each annealing step. At the same time, these curves became more and more symmetric because the thermal diffusion gradually made the top and bottom electrode interfaces the same. The capacitances in Fig. 8(b) decreased step by step after annealing and also became more symmetric at positive and negative dc biases. After annealing at 680 °C, the capacitance became hardly dependent on biased voltages, indicating that the sample has changed from semiconductor into insulator. On the other side, all these results support our

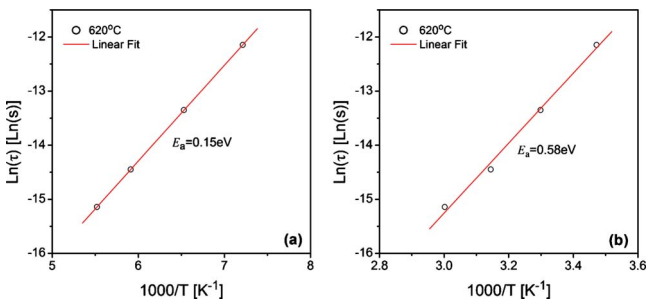

FIG. 6. (Color online) The $\ln(\tau)$-$1/T$ relationships for the (a) low and (b) high temperature relaxations in the CCTO thin film annealed at 620 °C.

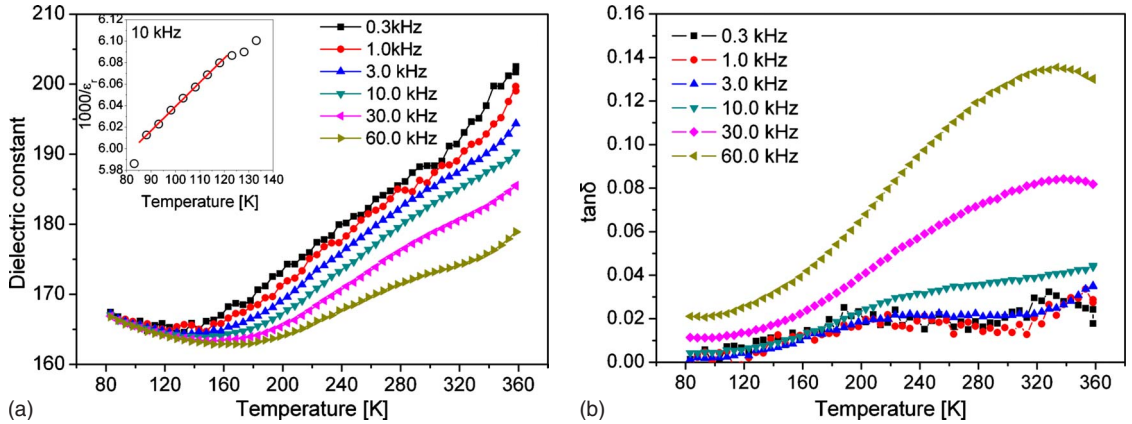

FIG. 7. (Color online) Temperature dependencies of (a) dielectric constant and (b) loss of the CCTO thin film annealed at 680 °C, and the inset is the $1/\varepsilon_r$-T curve.

previous finding that the top and bottom interfaces have different contact modes in the as-deposited sample.

Figure 9 shows the impedance spectroscopy of the as-deposited and annealed samples at RT. All of them show a single semicircle with two intercepts on the x axis. The high-frequency one is very close to the origin and the low-frequency one is on the right, and both of them are dependent on the annealing temperature. Raising annealing temperature, the former moved slightly to the right while the latter increased with orders of magnitude. These impedance results can be understood according to an equivalent circuit shown in Fig. 9. Even though the surface and bulk of the samples contributed to the conduction, the second semicircle did not show up because of the highly conductive bulk with low capacitance at room temperature. This feature has been observed in ceramic samples at room temperature by Sinclair *et al.*[4] After annealing, the resistance of the bulk increase and the high-frequency intercept shift to the right. However, it did not increase that much because the surface layer became thick and the bulk shrank at the same time due to the reduction in the impurity density. The whole resistance through the sample increased from 10^5 to 10^7 Ω when increasing annealing temperature from 480 to 620 °C. It can be roughly estimated in the range of 10^8–10^9 Ω after annealing at 680 °C.

Table I shows the estimated impurity densities after each annealing step derived from the IV curves. For the as-deposited annealed sample at 480 and 580 °C, we used the calculation method described in the first section. For the sample annealed at 620 °C, we adopted the method of "double Schottky barrier" described in Ref. 15 since the contacts at the top and bottom interfaces have become nearly symmetric. The results show that the impurity density was considerably reduced by annealing, changing from 1.5×10^{19} cm^{-3} after annealing at 480 °C to a low value of 2.4×10^{11} cm^{-3} after annealing at 620 °C. The impurity density after annealing at 680 °C could not be calculated due to the too low value of current density. The higher resistance at this state indicates an even lower impurity density. The table also shows that the characteristic relaxation time τ_0 gradually decreased after each annealing step. The corresponding data from the previous publication were listed in this table for comparison.

C. Discussion

The annealing experiments in this work make it clear that there was a second relaxation process which has higher activation energy than the well-known low-temperature relaxation process in CCTO. Both relaxation phenomena must be

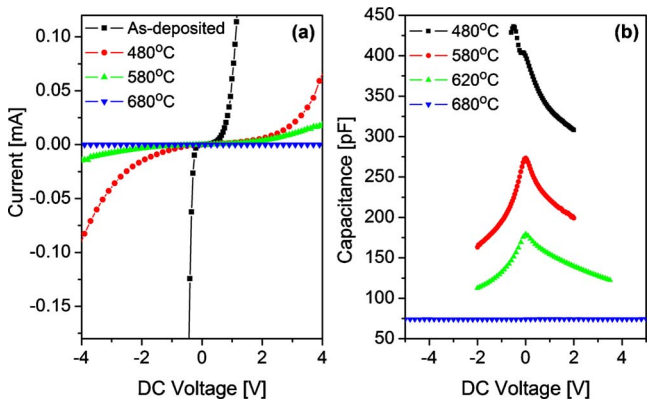

FIG. 8. (Color online) (a) I-V curve and (b) C^{-2}-V curve of the CCTO thin film annealed at different temperatures.

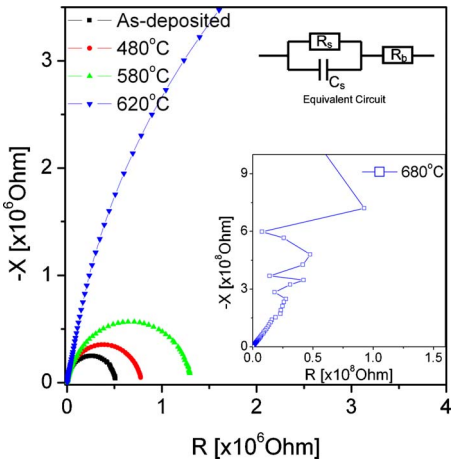

FIG. 9. (Color online) Impedance complex plane plot (20 Hz–1 MHz) of the CCTO thin film annealed at different temperatures.

related to oxygen vacancies since both of them decreased or disappeared after annealing in air. How to understand the two stepwise increases in the ε_r-T curve? The reported admittance spectroscopy results for semiconductor p-n or Schottky junctions may shed light on this question. For example, Seymour *et al.*[21] reported on capacitance-temperature spectroscopy of CdTe metal contacts, showing two so-called relaxation (steplike) processes at two different temperature ranges. They attributed these two relaxations to the two deep level trap states with different energy levels. Losee[12] theoretically and experimentally investigated the application of admittance spectroscopy in determining impurity levels in Schottky barriers. He explained multisteplike relaxations in the capacitance-temperature curves of Au-ZnTe samples based on several types of defect levels in the Schottky barrier. Vincent *et al.*[11] proposed another similar simpler model to successfully explain the capacitance-temperature data observed in GaP Schottky barriers. Here we adopt Vincent's model to simulate the capacitance response of our sample. According to this model, the capacitance of a Schottky junction is

$$C = A\left(\frac{\varepsilon q N_A^-}{2\phi}\right)^{1/2}\left(1 + \frac{N_A}{p}\frac{e_p^2}{e_p^2+\omega^2}\right). \quad (2)$$

A is the area of the junction, ε the dielectric constant of semiconductor, q the electron charge, N_A^- the concentration of ionized acceptor, N_A the doped acceptor concentration, p the hole carrier concentration on valence band, ϕ the band bending, ω the frequency, and e_p the hole emission rate. Among them, N_A^-, p, and e_p are the function of temperature. N_A^- and p can be determined after we get the Fermi level at each temperature and e_p can be calculated using the following equation:

$$e_p = e_{p0}\exp\left(\frac{E_a - E_V}{kT}\right). \quad (3)$$

e_{p0} is the pre-exponential constant, E_a the acceptor energy level, E_V the valence-band level, k the Boltzmann constant, and T the temperature.

This model indicated that the capacitance in the depletion layer is predominately determined by the charge emission or capture on trap levels due to the Fermi-level variation caused by the external ac signal. Therefore, the capacitance contribution of the different traps in the depletion layer can be simply considered as in parallel. The serial resistance was discussed by Vincent as well.[11] On the basis of their analysis, the serial resistance is small and can be neglected at the temperature range higher than the carrier freeze-out temperature. Even below this temperature, in fact, the serial resistance plays only a very limited role because the depletion layer width substantially increases and the bulk resistance decreases correspondingly. Their simulated result was very close to the measured results, confirming the above analysis.

In our simulation, we assume that CCTO contains two different acceptors with energy levels 0.10 and 0.50 eV higher than valence band, and concentration of 2×10^{17} cm^{-3} and 8×10^{16} cm^{-3}, respectively. We chose reasonable values for band gap (E_g=2.8 eV), acceptor density of states ($N_V=8\times10^{19}$ cm^{-3}), dielectric constant (ε_r=75), and diffusion potential of the band bending (Φ=0.8 eV), and apply the geometry of the measured sample. For the first step of the simulation, we calculated the Fermi level at each temperature step by using Poisson's equation and the numerical method. With the value of Fermi level, the concentration of charges (p and n) can be obtained. Thus, for different temperatures, we calculated the whole capacitance by summing the capacitance contribution [by Eq. (2)] from of each defect and the low-temperature capacitance limit C_0, which can be calculated by treating the whole junction as a parallel capacitor. The simulated capacitance and loss curves as a function of temperature are shown in Fig. 10.

The curves in Fig. 10(a) possess quite similar steplike relaxation and frequency-dependent features at the corresponding temperature ranges, and the dielectric losses in Fig. 10(b) show the corresponding relaxation peaks. Experimental results exhibit much more gradual transitions in the curves probably because of the broader distribution of impurities than theoretical simulation. The simulated results confirmed our previous speculation that the observed two relaxations in CCTO were caused by two defect energy levels: a shallower level and a deeper level, which correspond to D_{LT} and D_{HT}, respectively.

There are many reports concerning about the low-temperature relaxation process in CCTO. The E_a values of this relaxation ranged from 60 to 100 meV for various as-produced CCTO ceramics,[22] single crystal,[2] and thin films.[9] The E_a value observed in our work was ~87 meV for the as-deposited sample, consistent with the reported one. Such a consistence implies that the low-temperature relaxation observed in these samples have a common origin—the same shallow defect, namely, D_{LT}. And this defect is always ready to come into form during conventional synthesis procedures such as solid-state reaction, crystal growth, thin-film deposition, etc. The experimental results show that the energy level (or E_a) of D_{LT} can be changed by annealing. The activation energy of D_{LT} increased from 60 to 150 meV when raising the annealing temperature. This can be explained as follow-

TABLE I. Estimated impurity density in the CCTO thin film annealed at different temperatures.

Samples	As-deposited	480 °C	580 °C	620 °C	Single crystal[a]	Ceramics[b]
Impurity density (cm^{-3})	4.7×10^{19}	1.5×10^{19}	5.88×10^{18}	2.4×10^{11}		
Activation energy E_a (eV)	0.087	0.128	0.132	0.153	0.058	0.08
Relaxation time τ_0 (s)	2.78×10^{-9}	1.8×10^{-10}	2.85×10^{-10}	1.1×10^{-11}	8.9×10^{-8}	1.1×10^{-12}

[a]Reference 2.
[b]Reference 4.

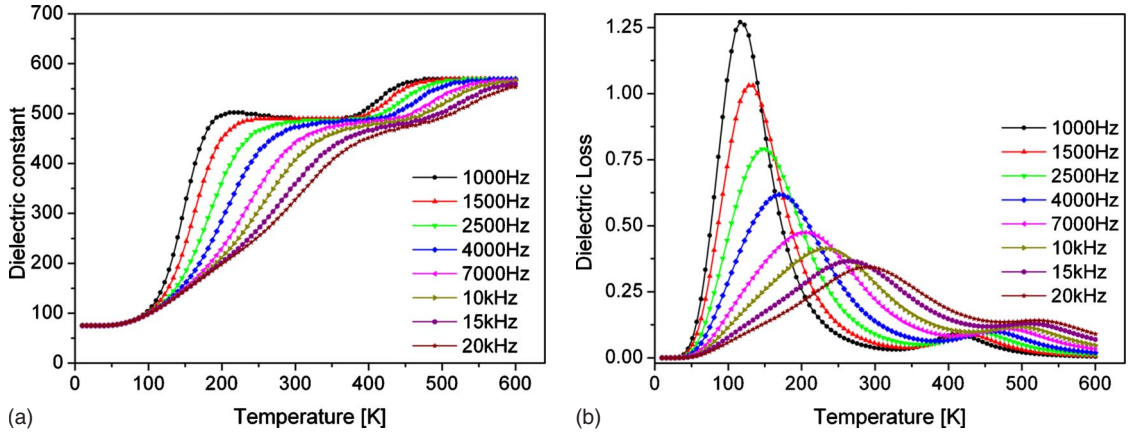

FIG. 10. (Color online) Simulated (a) dielectric constant and (b) loss of a CCTO Schottky junction containing two different defects.

ing: the increase in defect concentration results in a wider energy band of the acceptor level, which consequently reduces the gap between the bottom of the defect energy band and the top of the valence band. The similar doping effects on activation energy has been reported in boron-doped diamond films.[23] From this point of view, the reported as-produced CCTO samples (ceramics, single crystals, and thin films) had a high defect concentration because they had quite low activation energy. According to the E_a value from the sample annealed at 620 °C, which has very low defect concentration, D_{LT} should locate at an energy level around ~150 meV higher than the valence band of CCTO.

Our previous research showed that D_{LT} was related with the Cu-O sublattice.[6] As reported in literatures, copper oxides, CuO, and Cu_2O always contain some intrinsic acceptor defects of shallow energy levels (0.06–0.3 eV). For example, Serin *et al.*[24] observed an activation energy ~60 meV in CuO thin films. Jeong and Choi[25] obtained 100 meV activation energy in CuO powder. And G. P. Pollack and Trivich[26] measured 160 meV acceptor energy level by Hall measurement in CuO_2. Li-doped CuO ($Cu_{1-x}Li_xO$) have activation energy of 73 meV.[27] The as-produced CCTO sample includes Cu^{2+} and Cu^{+} at the same time, and they have the same square coordination with O as CuO.[6] Therefore, CCTO probably contains similar defects, which locate at the same energy-level range.

A clear picture of defect chemistry leading to *p*-type conduction with oxygen vacancies in CCTO is still missing. We may propose a possible explanation on the basis of Cu-O sublattice in CCTO. The possible reaction in synthesis and annealing of CCTO is

$$4Cu_{Cu}^{2+} + O_O \leftrightarrow 4(Cu_{Cu}^{+})' + \frac{1}{2}O_2 + V_O^{\bullet\bullet} + 2h^{\bullet}. \quad (4)$$

During the synthesis procedure at high temperature (for ceramic samples) or low oxygen pressure (for thin-film samples), Cu^{+} is favorable and the reaction goes to the right creating oxygen vacancies. When annealing in air at intermediate temperature, Cu^{2+} is more favorable and oxygen in the environment forces the equation to move back to the left, reducing the oxygen vacancies in the CCTO lattice.

As described above, D_{LT} was observed in almost all reported samples and played the main role in CDC while D_{HT} was not well discussed in the literature. Wang *et al.* reported relaxation peaks in dielectric loss spectra at ~250 K in the as-produced and N_2-annealed CCTO ceramic samples.[28,29] The experiments conducted by Fang *et al.*[28] showed that annealing in N_2 magnified the second relaxation at low frequency while annealing in O_2 suppressed this relaxation. Krohns *et al.*[29] observed a second steplike increase in dielectric constant in low-frequency range in a CCTO single-crystal sample too. All these observations could be related to D_{HT}, which we are discussing here. Thus, we can safely conclude that D_{HT} *does* originally exist in CCTO samples, from ceramics to single crystals to thin films. D_{LT} and D_{HT} are the two main defects contributing to the conduction in CCTO and responsible for the observed CDC phenomena in CCTO.

According to Eq. (1), the depletion capacitance is proportional to the square root of the impurity density of the depletion layer. Thus, the apparent dielectric constant directly reflects the defect concentration in the material. We will discuss the evolution of the defects in CCTO on the basis of the observed dielectric data. From our experiments, D_{LT} was quite stable at RT since the dielectric constant did not change much after keeping at RT for a few weeks. This was also supported by the work of Krohns *et al.*[30] They found that the first relaxation of the ceramic sample polished in N_2 was not influenced by annealing at RT in air. Conversely, D_{HT} seemed not stable at RT. The polished ceramic sample showed the second relaxation, which became weaker after 48 h in air.[30] Joanni *et al.*[31] reported that the conductivity of CCTO thin films could be controlled by different gas environments at temperatures of ~200 °C, which was probably also related to D_{HT}.

The density of D_{LT} was much higher than that of D_{HT} in the as-deposited sample, resulting in the overwhelming low-temperature relaxation but the very weak second relaxation. After annealing at 480 °C, the population of D_{LT} was substantially reduced while D_{HT} decreased to a much less extent. The same must be true for the corresponding defect concentration. The subsequent annealing at 580 °C did not apparently change the concentration of D_{LT} but reduced slightly the concentration of D_{HT}. Such a difference can be understood as that the D_{LT} concentration possibly reached a low

saturated value after annealing at 480 °C while D_{HT} was only active at temperature higher than 480 °C. Annealing at 620 °C resulted in reductions in both the D_{LT} and D_{HT} concentrations. Finally, D_{LT} and D_{HT} reduced to such low values at 680 °C that the conductivity was substantially suppressed due to missing charge carriers. As a whole view, D_{LT} was not sensitive to annealing at RT, but very sensitive to annealing at $T \sim 480$ °C, while D_{HT} was only influenced by annealing at $T \sim 580$ °C. Both D_{LT} and D_{HT} defects were originated from oxygen vacancies since their concentration strongly dependent on oxygen environments.

Another fact we should not ignore is that long-time annealing at high temperature did not change the behavior of the ceramic samples. Actually, we did the similar annealing experiments in CCTO ceramic samples. The dielectric constant did not evidently change, consistent with the reported results.[32] This means the oxygen diffusion into CCTO lattices is blocked by some thermodynamic barrier as soon as the surface layer has been oxidized, resulting in a limited effective diffusion distance about few hundreds of nanometer through the bulk. This layer, which can be oxidized by oxygen, can be called as the "oxidizable layer." Until now, it is difficult to specify what the thermodynamic barrier is. Maybe, the perfect stoichiometric CCTO lattice is not energetically favorable and some intrinsic defects such as Schottky-Wagner disorders like those in NaCl (Ref. 33) can reduce the free energy of the system (keeping stoichiometric). Since the TiO_6 octahedra in CCTO are strongly tilted to accommodate the square planar coordinated Cu ions,[7] the perfect CCTO lattice possibly possesses higher free energy than the lattice containing some vacancies, such as copper and oxygen vacancies at the fabrication temperatures of CCTO. Thus, a highly oxidized layer only forms on the shallow surface, as an impenetrable shield to prevent the further diffusion of oxygen ions into deep bulk. This speculation was supported by the theoretical electronic structure study conducted by Matos and Walmsley.[34] Their calculation suggested that oxygen vacancies are easily formed in CCTO due to the low electronegativity of Ca.

IV. CONCLUSION

In this paper, we discuss the annealing effects on electrical properties of the CCTO thin film deposited by pulsed laser deposition. Experimental results showed that the as-deposited CCTO thin film contained quite high concentration of defects, resulting in conduction of CCTO thin films. These defects can be effectively reduced by annealing in air, indicating they are related to oxygen vacancies. The defect concentration, activation energy, and relaxation time changed with the increase in annealing temperatures. The ε_r-T curves after annealing have the common two-step feature, which was attributed to the two defects in the CCTO lattice. The corresponding energy level of these defects was determined from the activation energy of the two relaxation processes. The simulation based on the obtained experimental parameters confirmed our understanding to the dielectric behavior. After annealing at 680 °C, the conduction in CCTO could be completely suppressed. The intrinsic dielectric properties of CCTO were observed, showing a negative temperature dependency. This abnormal dielectric behavior could be related to the magnetic ordering in CCTO at low temperature. On the basis of annealing experiments, an oxidizable barrier layer model was proposed to explain the unavoidable CDC phenomenon in bulk CCTO samples and the appearance and disappearance of the second relaxation process.

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[1] A. P. Ramirez, M. A. Subramanian, M. Gardel, G. Blumberg, D. Li, T. Vogt, and S. M. Shapiro, Solid State Commun. **115**, 217 (2000).
[2] C. C. Homes, T. Vogt, S. M. Shapiro, S. Wakimoto, and A. P. Ramirez, Science **293**, 673 (2001).
[3] S. B. Fagan, A. G. Souza Filho, A. P. Ayala, and J. Mendes Filho, Phys. Rev. B **72**, 014106 (2005).
[4] D. C. Sinclair, T. B. Adams, F. D. Morrison, and A. R. West, Appl. Phys. Lett. **80**, 2153 (2002).
[5] W. Si, E. M. Cruz, P. D. Johnson, P. W. Barnes, P. Woodward, and A. P. Ramirez, Appl. Phys. Lett. **81**, 2056 (2002).
[6] G. Deng, N. Xanthopoulos, and P. Muralt, Appl. Phys. Lett. **92**, 172909 (2008).
[7] M. A. Subramanian and A. W. Sleight, Solid State Sci. **4**, 347 (2002).
[8] P. Lunkenheimer, V. Bobnar, A. V. Pronin, A. I. Ritus, A. A. Volkov, and A. Loidl, Phys. Rev. B **66**, 052105 (2002).
[9] G. Deng, T. Yamada, and P. Muralt, Appl. Phys. Lett. **91**, 202903 (2007).
[10] T. Ning, C. Chen, Y. Zhou, H. Lu, D. Zhang, H. Ming, and G. Yang, Appl. Phys. A: Mater. Sci. Process. **94**, 567 (2009).
[11] G. Vincent, D. Bois, and P. Pinard, J. Appl. Phys. **46**, 5173 (1975).
[12] D. L. Losee, J. Appl. Phys. **46**, 2204 (1975).
[13] S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981).
[14] E. A. Kafadaryan, K. Cho, and N. Wu, J. Appl. Phys. **96**, 6591 (2004).
[15] T. B. Adams, D. C. Sinclair, and A. R. West, Phys. Rev. B **73**, 094124 (2006).
[16] K. Sakai and T. Ikoma, Appl. Phys. A: Mater. Sci. Process. **5**, 165 (1974).
[17] Ch. Kant, T. Rudolf, F. Mayr, S. Krohns, P. Lunkenheimer, S. G. Ebbinghaus, and A. Loidl, Phys. Rev. B **77**, 045131 (2008).
[18] J. Hao, W. Si, X. X. Xi, R. Guo, A. S. Bhalla, and L. E. Cross, Appl. Phys. Lett. **76**, 3100 (2000).
[19] G. Lawes, A. P. Ramirez, C. M. Varma, and M. A. Subramanian, Phys. Rev. Lett. **91**, 257208 (2003).
[20] M. Li, A. Feteira, D. C. Sinclair, and A. R. West, Appl. Phys. Lett. **91**, 132911 (2007).
[21] F. H. Seymour, V. Kaydanov, and T. R. Ohno, J. Appl. Phys. **100**, 033710 (2006).
[22] D. Capsoni, M. Binia, V. Massarotti, G. Chiodelli, M. C. Moz-

zatic, and C. B. Azzoni, J. Solid State Chem. **177**, 4494 (2004).
[23] S.-H. Chen, C.-L. Chen, M.-H. Tsai, J. J. Shyu, and C.-F. Chena, J. Electrochem. Soc. **142**, L223 (1995).
[24] N. Serin, T. Serin, and S. Karadeniz, Semicond. Sci. Technol. **17**, 60 (2002).
[25] Y. K. Jeong and G. M. Choi, J. Phys. Chem. Solids **57**, 81 (1996).
[26] G. P. Pollack and D. Trivich, J. Appl. Phys. **46**, 163 (1975).
[27] A. Tselev, C. M. Brooks, S. M. Anlage, H. Zheng, L. Salamanca-Riba, R. Ramesh, and M. A. Subramanian, Phys. Rev. B **70**, 144101 (2004).
[28] L. Fang, M. Shen, and W. Cao, J. Appl. Phys. **95**, 6483 (2004).
[29] S. Krohns, P. Lunkenheimer, S. G. Ebbinghaus, and A. Loidl, J. Appl. Phys. **103**, 084107 (2008).
[30] S. Krohns, P. Lunkenheimer, S. G. Ebbinghaus, and A. Loidl, Appl. Phys. Lett. **91**, 022910 (2007).
[31] E. Joanni, R. Savu, P. R. Bueno, E. Longo, and J. A. Varela, Appl. Phys. Lett. **92**, 132110 (2008).
[32] C. C. Wang and L. W. Zhang, Phys. Rev. B **74**, 024106 (2006).
[33] J. Nölting, Angew. Chem., Int. Ed. Engl. **9**, 489 (1970).
[34] M. Matos and L. Walmsley, J. Phys.: Condens. Matter **18**, 1793 (2006).